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**Amendments to the claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of claims:**

Claim 1 (currently amended): A semiconductor package, comprising:

a substrate having a first side for disposing a plurality of conductive traces thereon, and a second side for forming a plurality of electrical connection terminals thereon;

at least one chip attached to the first side of the substrate and electrically connected to the conductive traces;

at least one passive device attached to the first side of the substrate and electrically connected to the conductive traces;

a flash-proof device attached to the first side of the substrate and formed with a cavity for receiving the chip and the passive device therein, wherein a distance in elevation from a top side of the flash-proof device to the first side of the substrate is made to be slightly greater than a depth of a molding cavity of a mold used in a molding process, and the flash-proof device has an outer sidewall aligned with a side edge of the substrate; and

an encapsulant formed by a molding compound for encapsulating the chip, the passive device, the flash-proof device and the substrate, wherein the second side of the substrate is exposed to outside of the encapsulant;

wherein by the elevation-to-depth arrangement of the flash-proof device and the molding cavity, the top side of the flash-proof device is exposed to outside of the encapsulant, and the second side of the substrate is free of flash of the molding compound.

Claim 2 (original): The semiconductor package of claim 1, wherein the flash-proof device is attached to the substrate by an elastic adhesive.

Claim 3 (original): The semiconductor package of claim 1, wherein the flash-proof device is attached to the substrate by a thermally conductive adhesive.

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**Claim 4 (previously presented):** The semiconductor package of claim 1, wherein the flash-proof device is further formed with a plurality of vias, which allow the molding compound used for forming the encapsulant to flow therethrough.

**Claim 5 (original):** The semiconductor package of claim 1, wherein a plurality of step-like recesses are formed on edges of the top side of the flash-proof device.

**Claim 6 (original):** The semiconductor package of claim 1, wherein the flash-proof device has an outer sidewall thereof adjacent to a side edge of the substrate.

**Claims 7-8 (canceled)**

**Claim 9 (original):** The semiconductor package of claim 1, wherein a plurality of ground traces are formed on the conductive traces at positions corresponding to the flash-proof device, for attaching the flash-proof device to the ground traces by using an electrically conductive adhesive.